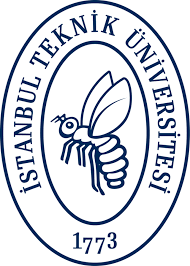
****

**DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E**

**Experiment II**

**Yiğit Bektaş GÜRSOY**

**040180063**

**Class Lecturer: Sıddıka Berna Örs Yalçın**

**Class Assistant:  
Serdar Duran  
Yasin Fırat Kula  
Mehmet Onur Demirtürk**

1. **DECODER**

* Truth table of a 4x16 Decoder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I3** | **I2** | **I1** | **I0** | **O0** | **O1** | **O2** | **O3** | **O4** | **O5** | **O6** | **O7** | **O8** | **O9** | **O10** | **O11** | **O12** | **O13** | **O14** | **O15** |
| **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

* DECODER Verilog code, testbench code and behavioral simulation wave screen-shots

**VERILOG CODE**

**module** Top\_Module**(**

**input** **[**7**:**0**]**SW**,**

**input** **[**3**:**0**]**BTN**,**

**output** **[**7**:**0**]**LED**,**

**output** **[**6**:**0**]**CAT**,**

**output** **[**3**:**0**]**AN**,**

**output** **[**0**:**0**]**DP

**);**

DECODER DECODER1**(**

**.**IN**(**SW**[**3**:**0**]),**

**.**OUT**({**DP**,**CAT**,**LED**})**

**);**

**assign** AN **=** 4'b1110**;**

**module** DECODER **(**

**input** **[**3**:**0**]**IN**,**

**output** **reg** **[**15**:**0**]**OUT

**);**

**always** **@(**IN**)**

**begin**

**case(**IN**)**

4'b0000**:** OUT **=** 16'b0000\_0000\_0000\_0001**;**

4'b0001**:** OUT **=** 16'b0000\_0000\_0000\_0010**;**

4'b0010**:** OUT **=** 16'b0000\_0000\_0000\_0100**;**

4'b0011**:** OUT **=** 16'b0000\_0000\_0000\_1000**;**

4'b0100**:** OUT **=** 16'b0000\_0000\_0001\_0000**;**

4'b0101**:** OUT **=** 16'b0000\_0000\_0010\_0000**;**

4'b0110**:** OUT **=** 16'b0000\_0000\_0100\_0000**;**

4'b0111**:** OUT **=** 16'b0000\_0000\_1000\_0000**;**

4'b1000**:** OUT **=** 16'b0000\_0001\_0000\_0000**;**

4'b1001**:** OUT **=** 16'b0000\_0010\_0000\_0000**;**

4'b1010**:** OUT **=** 16'b0000\_0100\_0000\_0000**;**

4'b1011**:** OUT **=** 16'b0000\_1000\_0000\_0000**;**

4'b1100**:** OUT **=** 16'b0001\_0000\_0000\_0000**;**

4'b1101**:** OUT **=** 16'b0010\_0000\_0000\_0000**;**

4'b1110**:** OUT **=** 16'b0100\_0000\_0000\_0000**;**

4'b1111**:** OUT **=** 16'b1000\_0000\_0000\_0000**;**

**endcase**

**end**

**endmodule**

**TEST BENCH CODE**

`timescale 1ns **/** 1ps

**module** Top\_Module\_tb**();**

**reg** **[**7**:**0**]**SW**;**

**reg** **[**3**:**0**]**BTN**;**

**wire** **[**7**:**0**]**LED**;**

**wire** **[**6**:**0**]**CAT**;**

**wire** **[**3**:**0**]**AN**;**

**wire** **[**0**:**0**]**DP**;**

Top\_Module DUT**(**

**.**SW**(**SW**),**

**.**BTN**(**BTN**),**

**.**LED**(**LED**),**

**.**CAT**(**CAT**),**

**.**AN**(**AN**),**

**.**DP**(**DP**)**

**);**

**initial**

**begin**

SW**[**3**:**0**]** **=** 4'h0**;**

**#**10 SW**[**3**:**0**]** **=** 4'h1**;**

**#**10 SW**[**3**:**0**]** **=** 4'h2**;**

**#**10 SW**[**3**:**0**]** **=** 4'h3**;**

**#**10 SW**[**3**:**0**]** **=** 4'h4**;**

**#**10 SW**[**3**:**0**]** **=** 4'h5**;**

**#**10 SW**[**3**:**0**]** **=** 4'h6**;**

**#**10 SW**[**3**:**0**]** **=** 4'h7**;**

**#**10 SW**[**3**:**0**]** **=** 4'h8**;**

**#**10 SW**[**3**:**0**]** **=** 4'h9**;**

**#**10 SW**[**3**:**0**]** **=** 4'hA**;**

**#**10 SW**[**3**:**0**]** **=** 4'hB**;**

**#**10 SW**[**3**:**0**]** **=** 4'hC**;**

**#**10 SW**[**3**:**0**]** **=** 4'hD**;**

**#**10 SW**[**3**:**0**]** **=** 4'hE**;**

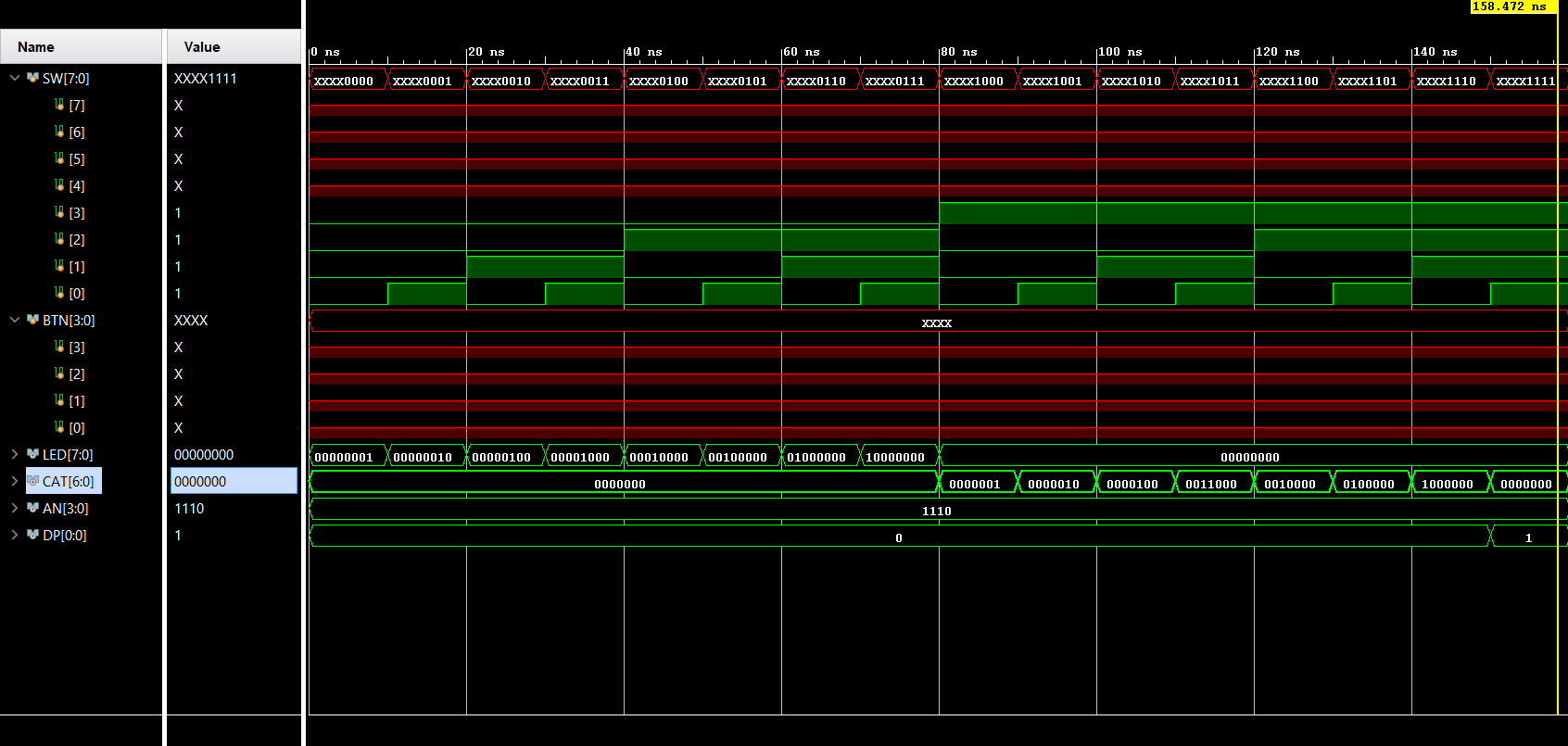
**#**10 SW**[**3**:**0**]** **=** 4'hF**;**

**#**10 $finish**;**

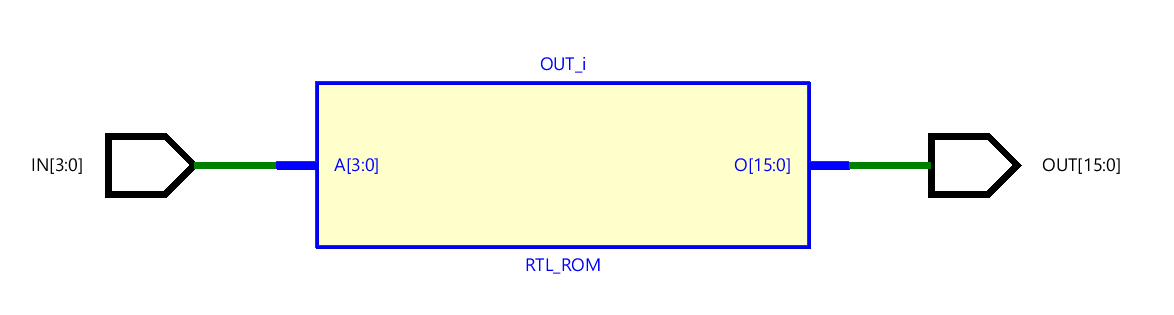
**end**

**endmodule**

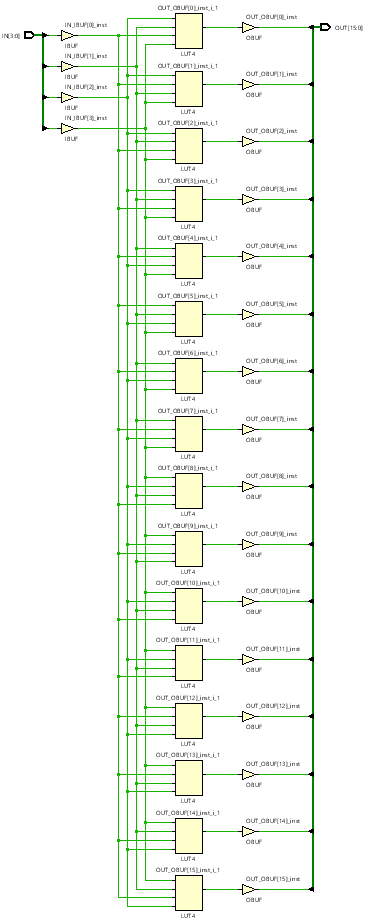
**BEHAVIORAL SIMULATION**

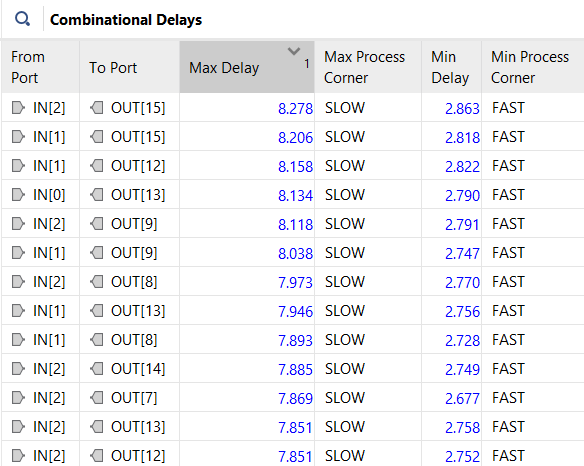
****

* RTL schematic

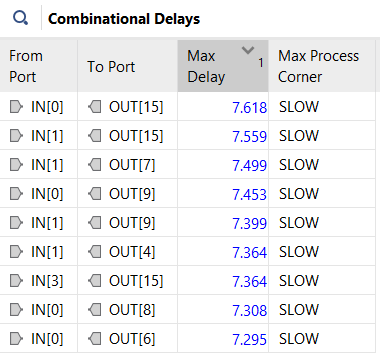
****

* Technology Schematic

****

* As seen in the technology schematic, we have 16 LUT4s. There are 16 different logic expressions in the diagram. Except for the bit that corresponds to the output of LUT4, the other inputs take the value 0 (corresponding to 0101 ==> 5th output). Under these conditions, LUT4 gets 1 in its logical expression. Combining LUTs this way creates the decoder.
* ****Greates Delay of Decoder

* Greatest delay of the implemented design is 8.278ns.
* Greatest Delay of Decoder After Timing Constrait



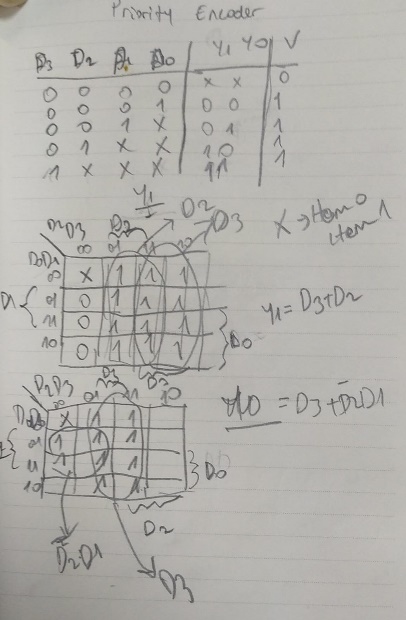
* Instead of the 10ns delay written on the leaflet, I observed 8.278ns delay. Then I set the maximum delay to 8ns from the edit timing constraint part. The relevant results are indicated in the photo above.

1. **PRIORITY ENCODER**

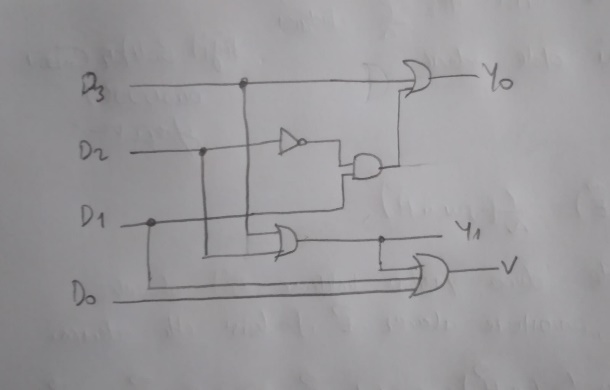
* Truth Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **D3** | **D2** | **D1** | **D0** | **OUT0** | **OUT1** | **V** |
| **0** | **0** | **0** | **0** | **X** | **X** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **0** | **1** | **X** | **0** | **1** | **1** |
| **0** | **1** | **X** | **X** | **1** | **0** | **1** |
| **1** | **X** | **X** | **X** | **1** | **1** | **1** |

* Karnaugh Map



* Hand Drawn Schematic



**VERILOG CODE**

**module** Top\_Module**(**

**input** **[**7**:**0**]**SW**,**

**input** **[**3**:**0**]**BTN**,**

**output** **[**7**:**0**]**LED**,**

**output** **[**6**:**0**]**CAT**,**

**output** **[**3**:**0**]**AN**,**

**output** **[**0**:**0**]**DP

**);**

ENCODER ENCODER1**(**

**.**IN**(**SW**[**3**:**0**]),**

**.**OUT**(**LED**[**1**:**0**]),**

**.**V**(**LED**[**7**])**

**);**

**module** ENCODER**(**

**input** **[**3**:**0**]**IN**,**

**output** **[**1**:**0**]**OUT**,**

**output** **[**0**:**0**]**V

**);**

**assign** OUT**[**0**]** **=** **(**IN**[**3**])** **|** **(**IN**[**1**]** **&** **~(**IN**[**2**]));**

**assign** OUT**[**1**]** **=** IN**[**3**]** **|** IN**[**2**];**

**assign** V **=** **(**IN**[**0**])** **|** **(**IN**[**1**])** **|** **(**IN**[**2**])** **|** **(**IN**[**3**]);**

**endmodule**

**TESTBENCH CODE**

**module** Top\_Module\_tb**();**

**reg** **[**7**:**0**]**SW**;**

**reg** **[**3**:**0**]**BTN**;**

**wire** **[**7**:**0**]**LED**;**

**wire** **[**6**:**0**]**CAT**;**

**wire** **[**3**:**0**]**AN**;**

**wire** **[**0**:**0**]**DP**;**

Top\_Module DUT**(**

**.**SW**(**SW**),**

**.**BTN**(**BTN**),**

**.**LED**(**LED**),**

**.**CAT**(**CAT**),**

**.**AN**(**AN**),**

**.**DP**(**DP**)**

**);**

**initial**

**begin**

SW**[**3**:**0**]** **=** 4'h0**;**

**#**10 SW**[**3**:**0**]** **=** 4'h1**;**

**#**10 SW**[**3**:**0**]** **=** 4'h2**;**

**#**10 SW**[**3**:**0**]** **=** 4'h3**;**

**#**10 SW**[**3**:**0**]** **=** 4'h4**;**

**#**10 SW**[**3**:**0**]** **=** 4'h5**;**

**#**10 SW**[**3**:**0**]** **=** 4'h6**;**

**#**10 SW**[**3**:**0**]** **=** 4'h7**;**

**#**10 SW**[**3**:**0**]** **=** 4'h8**;**

**#**10 SW**[**3**:**0**]** **=** 4'h9**;**

**#**10 SW**[**3**:**0**]** **=** 4'hA**;**

**#**10 SW**[**3**:**0**]** **=** 4'hB**;**

**#**10 SW**[**3**:**0**]** **=** 4'hC**;**

**#**10 SW**[**3**:**0**]** **=** 4'hD**;**

**#**10 SW**[**3**:**0**]** **=** 4'hE**;**

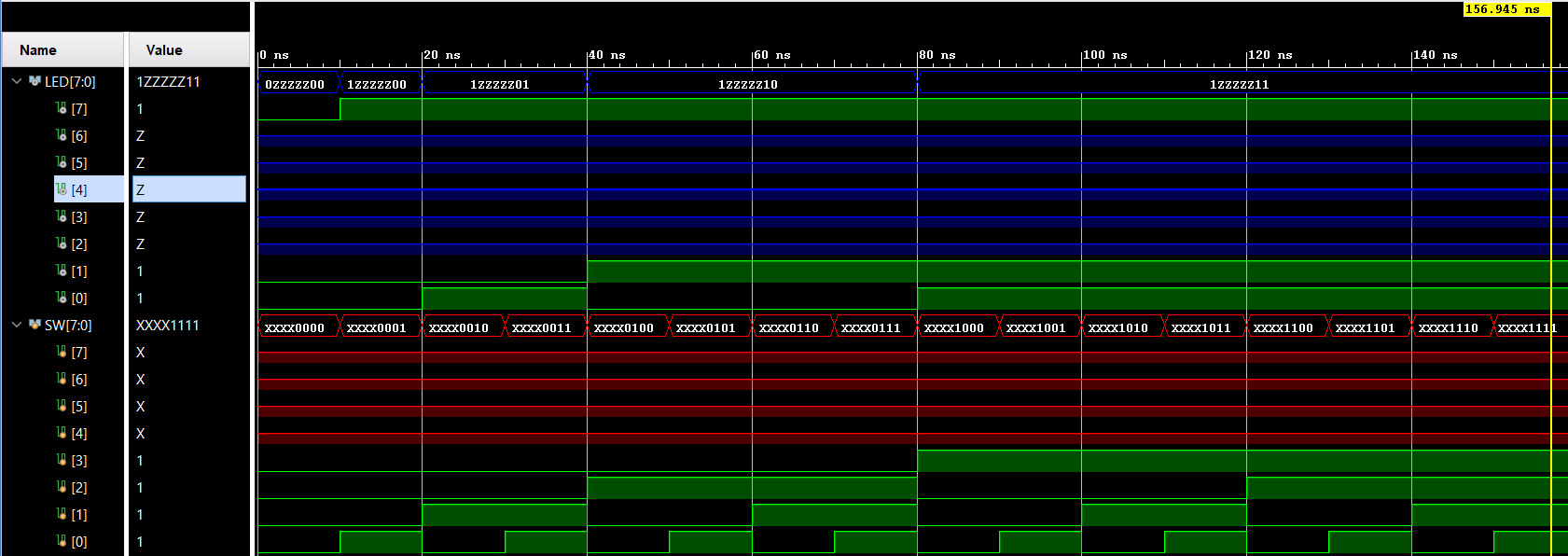
**#**10 SW**[**3**:**0**]** **=** 4'hF**;**

**#**10 $finish**;**

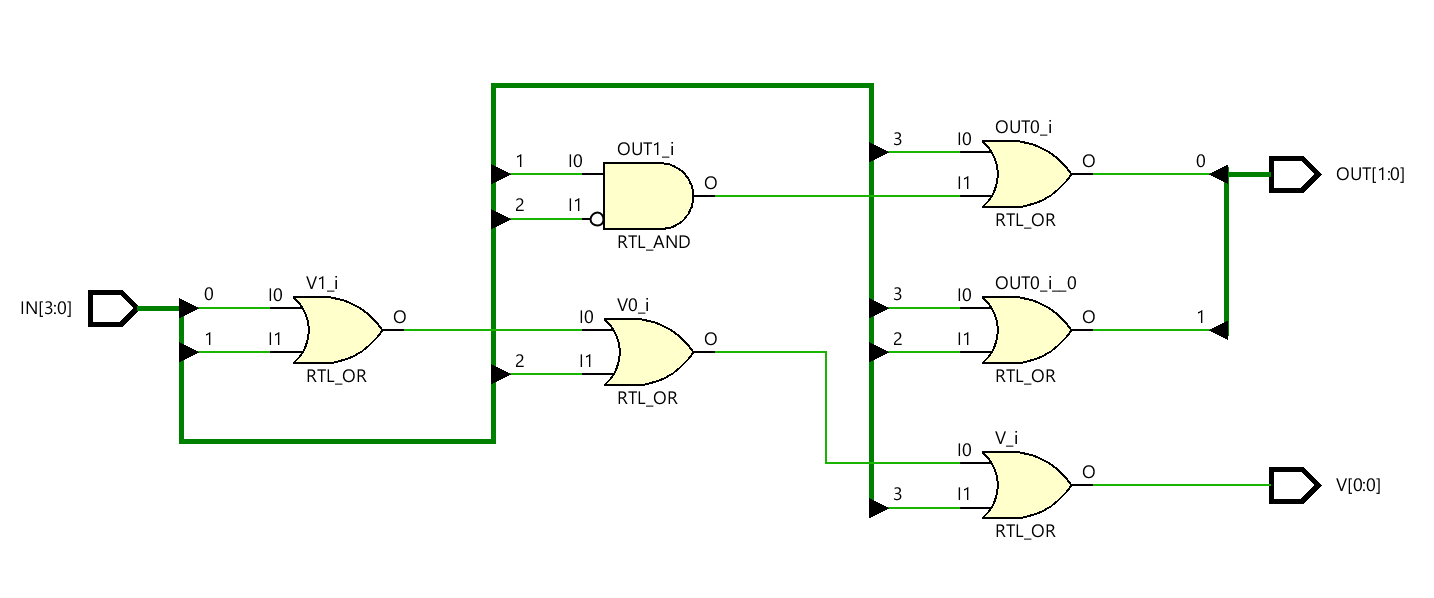
**end**

**endmodule**

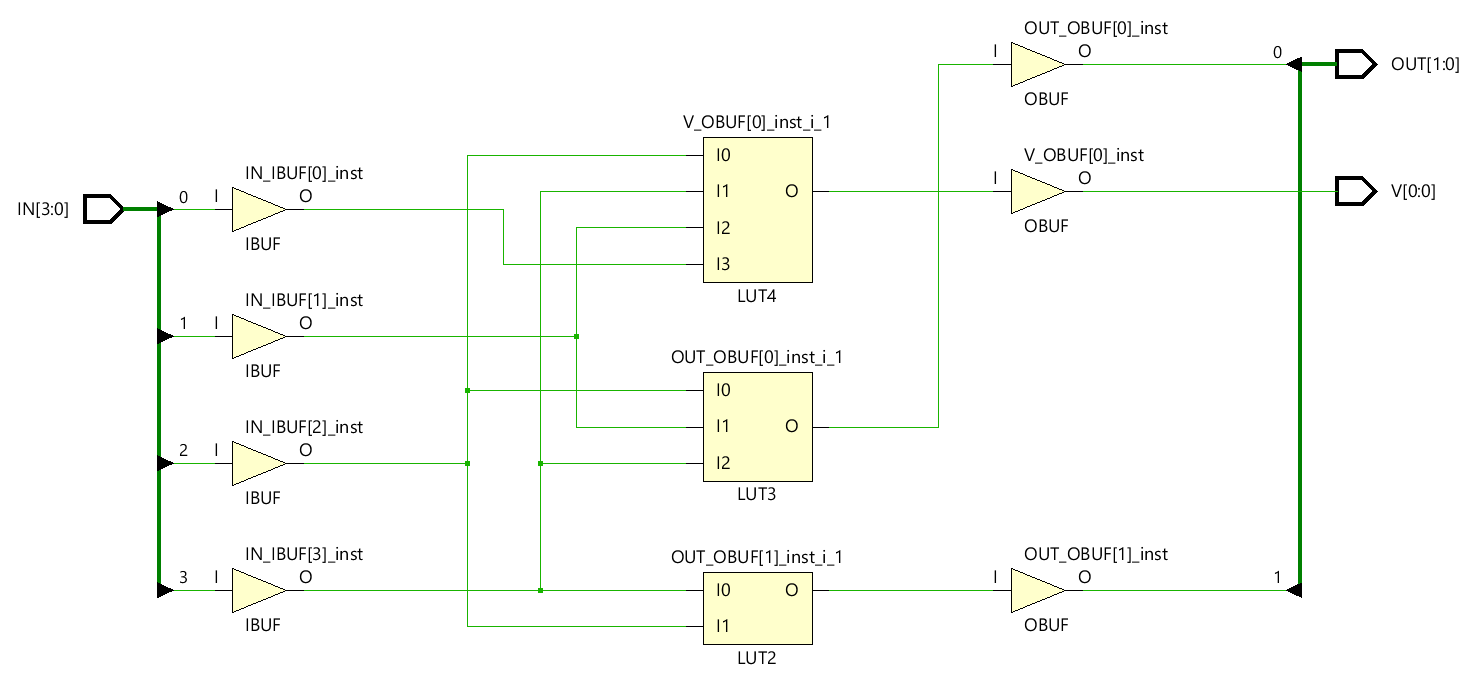
**BEHAVIORAL SIMULATION**

****

* RTL schematic

****

* Technology schematic

****

* 5 or gate 1 and gate and 1 note gate are used as seen in the RTL schematic. Total of 7 transactions were made.
* In the technology schematic, LUT4, LUT3 and LUT2 are used. They were accompanied by 4 buffers at their entrances and 3 buffers at their exits. A total of 7 buffers were used.

**VERILOG CODE**

**(Case Structure of Encoder)**

**module** ENCODER**(**

**input** **[**3**:**0**]**IN**,**

**output** **reg** **[**1**:**0**]**OUT**,**

**output** **reg** **[**0**:**0**]**V

**);**

**always@(**IN**)**

**begin**

**casez** **(**IN**)**

4'b0000**:**

**begin**

OUT **=** 2'b??**;**

V **=** 1'b0**;**

**end**

4'b0001**:**

**begin**

OUT **=** 2'b00**;**

V **=** 1'b1**;**

**end**

4'b001?**:**

**begin**

OUT **=** 2'b01**;**

V **=** 1'b1**;**

**end**

4'b01??**:**

**begin**

OUT **=** 2'b10**;**

V **=** 1'b1**;**

**end**

4'b1???**:**

**begin**

OUT **=** 2'b11**;**

V **=** 1'b1**;**

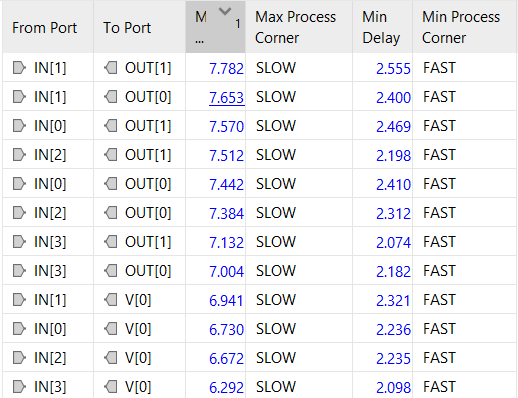
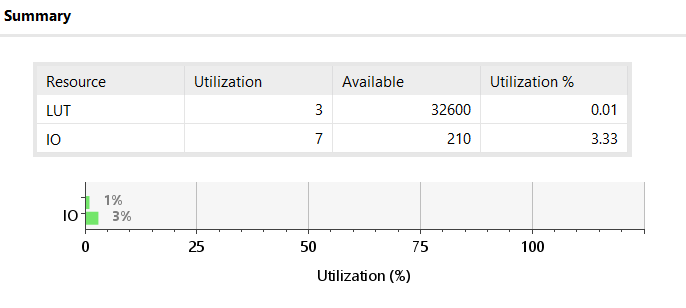
**end**

**endcase**

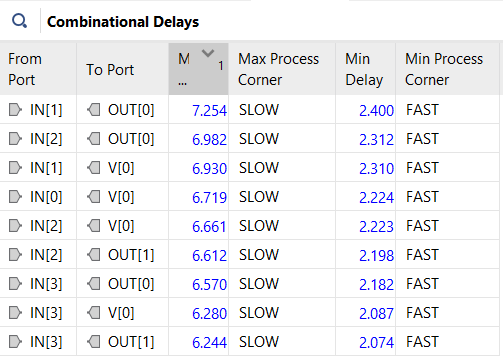
**end**

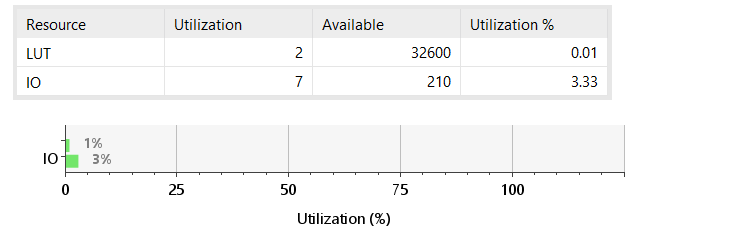
**endmodule**

* Implementation results
* Timing and utilization report of the behavioral design.



* Timing and utilization report of the structural design.

****

****

* There is a serious difference between the field uses that are not suitable for general use. It performs better in behavioral designs than in delay performances. They have less delays than behavioral designs.

1. **MULTIPLEXER**

**VERILOG CODE**

**module** Top\_Module**(**

**input** **[**7**:**0**]**SW**,**

**input** **[**3**:**0**]**BTN**,**

**output** **[**7**:**0**]**LED**,**

**output** **[**6**:**0**]**CAT**,**

**output** **[**3**:**0**]**AN**,**

**output** **[**0**:**0**]**DP

**);**

MUX MUX1**(**

**.**D**(**SW**[**3**:**0**]),**

**.**S**(**BTN**[**1**:**0**]),**

**.**O**(**LED**[**0**]));**

**module** MUX**(**

**input** **[**3**:**0**]**D**,**

**input** **[**1**:**0**]**S**,**

**output** **reg** **[**0**:**0**]**O**);**

**wire** y0**,**y1**,**y2**,**y3**;**

**assign** y0 **=** D**[**0**]** **&&** **~**S**[**0**]** **&&** **~**S**[**1**];**

**assign** y1 **=** D**[**1**]** **&&** **~**S**[**0**]** **&&** S**[**1**];**

**assign** y2 **=** D**[**2**]** **&&** S**[**0**]** **&&** **~**S**[**1**];**

**assign** y3 **=** D**[**3**]** **&&** S**[**0**]** **&&** S**[**1**];**

**assign** O **=** y0 **||** y1 **||** y2 **||** y3**;**

**endmodule**

**TESTBENCH CODE**

**module** Top\_Module\_tb**();**

**reg** **[**7**:**0**]**SW**;**

**reg** **[**3**:**0**]**BTN**;**

**wire** **[**7**:**0**]**LED**;**

**wire** **[**6**:**0**]**CAT**;**

**wire** **[**3**:**0**]**AN**;**

**wire** **[**0**:**0**]**DP**;**

Top\_Module DUT**(**

**.**SW**(**SW**),**

**.**BTN**(**BTN**),**

**.**LED**(**LED**),**

**.**CAT**(**CAT**),**

**.**AN**(**AN**),**

**.**DP**(**DP**)**

**);**

**initial**

**begin**

SW**[**3**:**0**]** **=** 4'b0000**;** **#**10 BTN**[**2**:**0**]** **=** 2'h0 **;#**10 BTN**[**2**:**0**]** **=** 2'h1 **;#**10 BTN**[**2**:**0**]** **=** 2'h2 **;#**10 BTN**[**2**:**0**]** **=** 2'h3 **;**

**#**10 SW**[**3**:**0**]** **=** 4'b0001**;** **#**10 BTN**[**2**:**0**]** **=** 2'h0 **;#**10 BTN**[**2**:**0**]** **=** 2'h1 **;#**10 BTN**[**2**:**0**]** **=** 2'h2 **;#**10 BTN**[**2**:**0**]** **=** 2'h3 **;**

**#**10 SW**[**3**:**0**]** **=** 4'b0010**;** **#**10 BTN**[**2**:**0**]** **=** 2'h0 **;#**10 BTN**[**2**:**0**]** **=** 2'h1 **;#**10 BTN**[**2**:**0**]** **=** 2'h2 **;#**10 BTN**[**2**:**0**]** **=** 2'h3 **;**

**#**10 SW**[**3**:**0**]** **=** 4'b0100**;** **#**10 BTN**[**2**:**0**]** **=** 2'h0 **;#**10 BTN**[**2**:**0**]** **=** 2'h1 **;#**10 BTN**[**2**:**0**]** **=** 2'h2 **;#**10 BTN**[**2**:**0**]** **=** 2'h3 **;**

**#**10 SW**[**3**:**0**]** **=** 4'b1000**;** **#**10 BTN**[**2**:**0**]** **=** 2'h0 **;#**10 BTN**[**2**:**0**]** **=** 2'h1 **;#**10 BTN**[**2**:**0**]** **=** 2'h2 **;#**10 BTN**[**2**:**0**]** **=** 2'h3 **;**

**#**10 $finish**;**

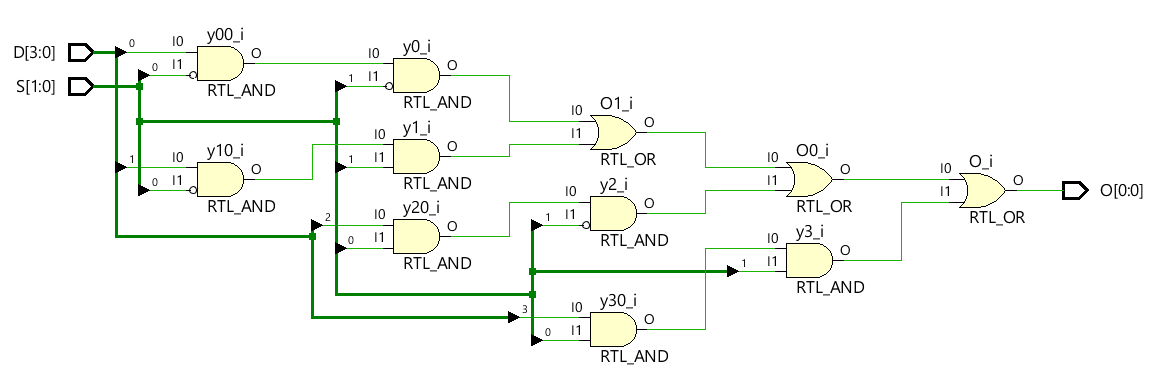
**end**

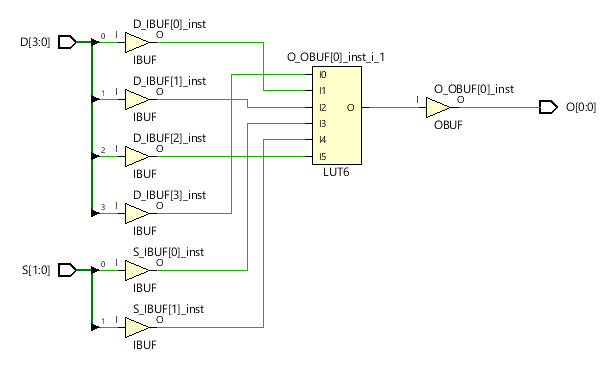
**endmodule**

**BEHAVIORAL SIMULATION**

****

* RTL schematic



* Technology schematic

**VERILOG CODE**

**(Case Structure of MUX)**

**module** MUX**(**

**input** **[**3**:**0**]**D**,**

**input** **[**1**:**0**]**S**,**

**output** **reg** **[**0**:**0**]**O**);**

**always** **@(**D**,**S**)**

**begin**

**case** **(**S**)**

2'b00**:** O **=** D**[**0**];**

2'b01**:** O **=** D**[**1**];**

2'b10**:** O **=** D**[**2**];**

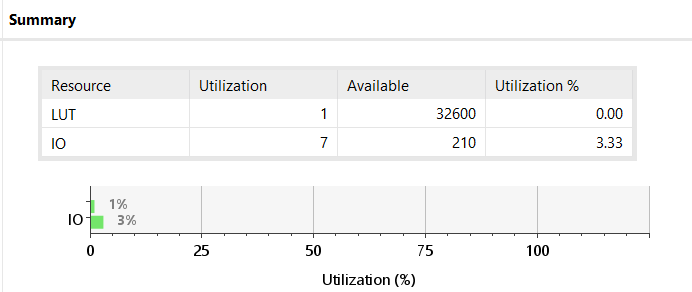
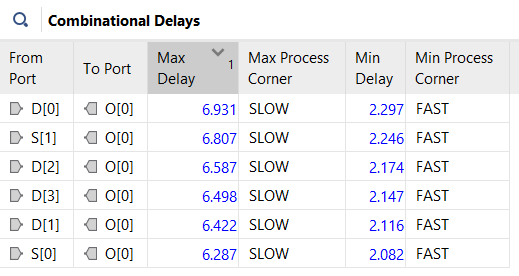
2'b11**:** O **=** D**[**3**];**

**endcase**

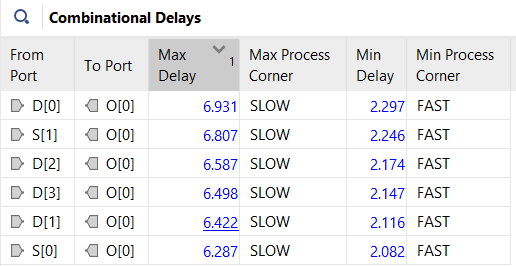
**end**

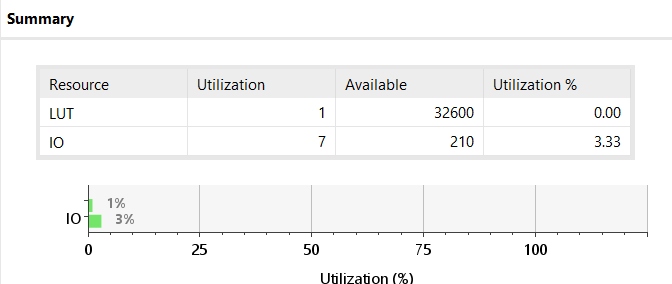
**endmodule**

* Implementation results
* Timing and utilization report of the behavioral design.

****

* Timing and utilization report of the structural design.



****

* Delay times and area are very similar in between structural and behavioral design.

1. **DEMULTIPLEXER**

**VERILOG CODE**

**module** Top\_Module**(**

**input** **[**7**:**0**]**SW**,**

**input** **[**3**:**0**]**BTN**,**

**output** **[**7**:**0**]**LED**,**

**output** **[**6**:**0**]**CAT**,**

**output** **[**3**:**0**]**AN**,**

**output** **[**0**:**0**]**DP

**);**

DEMUX DEMUX1**(**

**.**D**(**SW**[**0**]),**

**.**S**(**BTN**[**1**:**0**]),**

**.**O**(**LED**[**3**:**0**]));**

**endmodule**

**module** DEMUX**(**

**input** **[**0**:**0**]**D**,**

**input** **[**1**:**0**]**S**,**

**output** **[**3**:**0**]**O

**);**

**wire** s0\_not**,** s1\_not**;**

NOT\_gate NOT1**(.**I1**(**S**[**0**]),** **.**O**(**s0\_not**));**

NOT\_gate NOT2**(.**I1**(**S**[**1**]),** **.**O**(**s1\_not**));**

**wire** y0**,**y1**,**y2**,**y3**;**

AND\_gate AND1**(** **.**I1**(**s0\_not**),** **.**I2**(**s1\_not**),** **.**O**(**y0**));**

AND\_gate AND2**(** **.**I1**(**s0\_not**),** **.**I2**(**S**[**1**]),** **.**O**(**y1**));**

AND\_gate AND3**(** **.**I1**(**S**[**0**]),** **.**I2**(**s1\_not**),** **.**O**(**y2**));**

AND\_gate AND4**(** **.**I1**(**S**[**0**]),** **.**I2**(**S**[**1**]),** **.**O**(**y3**));**

TRI TRI1**(** **.**I**(**D**[**0**]),** **.**E**(**y0**),** **.**O**(**O**[**0**]));**

TRI TRI2**(** **.**I**(**D**[**0**]),** **.**E**(**y1**),** **.**O**(**O**[**1**]));**

TRI TRI3**(** **.**I**(**D**[**0**]),** **.**E**(**y2**),** **.**O**(**O**[**2**]));**

TRI TRI4**(** **.**I**(**D**[**0**]),** **.**E**(**y3**),** **.**O**(**O**[**3**]));**

**endmodule**

**TESTBENCH CODE**

**module** Top\_Module\_tb**();**

**reg** **[**7**:**0**]**SW**;**

**reg** **[**3**:**0**]**BTN**;**

**wire** **[**7**:**0**]**LED**;**

**wire** **[**6**:**0**]**CAT**;**

**wire** **[**3**:**0**]**AN**;**

**wire** **[**0**:**0**]**DP**;**

Top\_Module DUT**(**

**.**SW**(**SW**),**

**.**BTN**(**BTN**),**

**.**LED**(**LED**),**

**.**CAT**(**CAT**),**

**.**AN**(**AN**),**

**.**DP**(**DP**)**

**);**

**initial**

**begin**

SW**[**0**]=** 1'b0**;** **#**10 BTN**[**1**:**0**]** **=** 2'h0 **;#**10 BTN**[**1**:**0**]** **=** 2'h1 **;#**10 BTN**[**1**:**0**]** **=** 2'h2 **;#**10 BTN**[**1**:**0**]** **=** 2'h3**;**

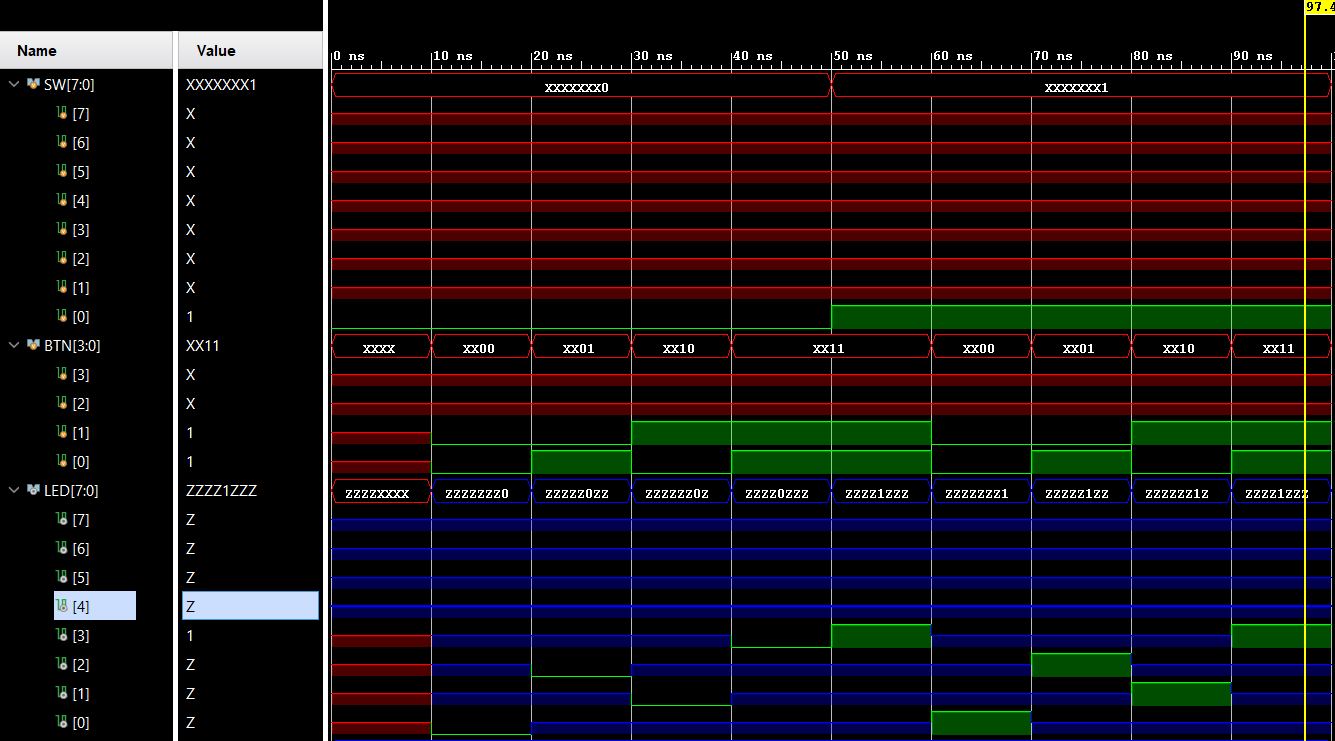
**#**10 SW**[**0**]=** 1'b1**;** **#**10 BTN**[**1**:**0**]** **=** 2'h0 **;#**10 BTN**[**1**:**0**]** **=** 2'h1 **;#**10 BTN**[**1**:**0**]** **=** 2'h2 **;#**10 BTN**[**1**:**0**]** **=** 2'h3**;**

**#**10 $finish**;**

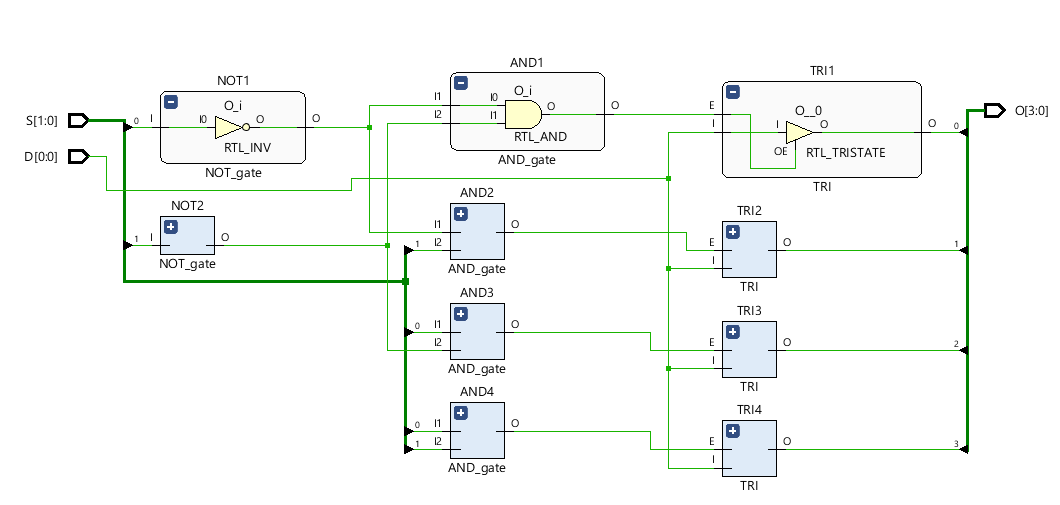
**end**

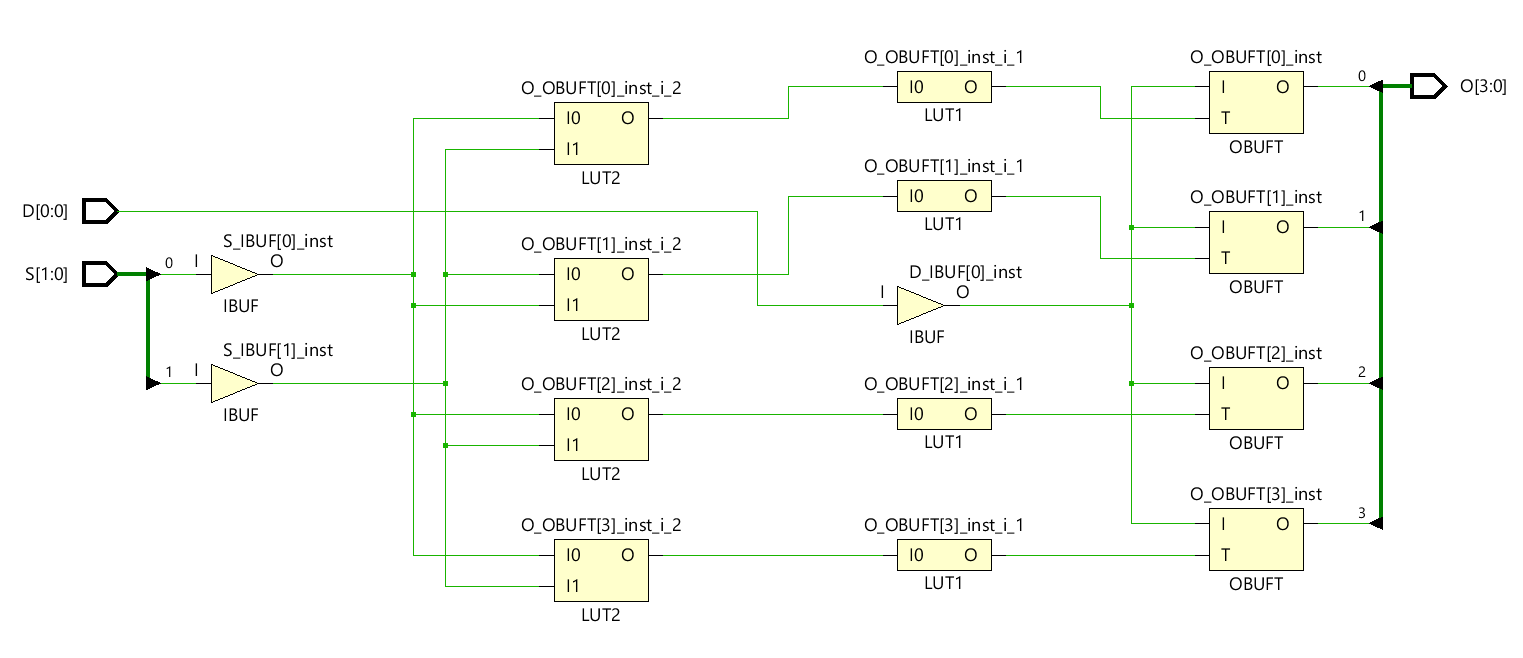
**endmodule**

**BEHAVIORAL SIMULATION**

****

* RTL schematic



* Technology schematic